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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,074	08/01/2003	David Wayne Self	P-0223	4239

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PATENT DEPARTMENT
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EXAMINER	
VAN ROY, TOD THOMAS	
ART UNIT	**PAPER NUMBER**
2828	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,074	Wayne et al.	
	Examiner	Art Unit	
	Tod T. Van Roy	2828	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 22* is/are rejected.

7)☒ Claim(s) *17-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: fig.3 #319, 321, 323, 325; fig.4 #419; fig.6 #519; and fig.13 #1300. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 10-12, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ciubotaru et al. (US 2003/0086455) in view of Grodevant (US 5666045).

With respect to claim 1, Ciubotaru teaches a driver circuit (fig.1) comprising a buffer circuit (fig.1 #10) for receiving a differential electrical signal, and a driver amplifier (fig.1 #12) having a first input coupled to the output of said buffer circuit and a second input coupled to a bias control (fig.1 #11) providing a precisely controlled waveform to an optoelectronic device (fig.1 #13). Ciubotaru does not teach the driver circuit to comprise a voltage regulator. Grodevant teaches a driver circuit (fig.1) comprising a voltage regulator (fig.1 #19) having an input adapted to receive a control signal and an output adapted to provide an output voltage that is a function of the control signal (col.20 lines 58- col.21 line 27). It would have been obvious to one of ordinary skill at the time of the invention to combine the driver circuit of Ciubotaru with the voltage regulator of Grodevant to supply a constant voltage to the optoelectronic device and allow for reliable operation (Grodevant, col.5 lines 43-46).

With respect to claim 2, Ciubotaru and Grodevant teach the driver circuit in the rejection to claim 1, and further teach the buffer circuit to comprise an attenuating input stage having a pair of resistors (Ciubotaru, fig.2 R1b and R2b) and an amplifying output stage (fig.2 Abuf).

With respect to claim 10, Ciubotaru and Grodevant teach the driver circuit in the rejection to claim 1, and further teach the system to comprise a laser diode (Ciubotaru, fig.1 #13).

With respect to claim 11, Ciubotaru and Grodevant teach the driver circuit in the rejection to claim 1, and further teach the laser diode to be a VCSEL (Ciubotaru, fig.1 #13).

With respect to claim 12, Ciubotaru and Grodevant teach the driver circuit in the rejection to claim 1, but do not teach duplicate components of the circuit. It would have been obvious to one of ordinary skill in the art at the time of the invention to add duplicate components to the existing system in order to achieve multiple outputs. MPEP 2144.04 IV b states mere duplication of parts has no patentable significance unless a new and unexpected result is produced, while in this claim the outcome would in fact produce no new or unexpected results as only the number of previously presented parts is being increased.

Claim 22 is rejected for the same reasons as claim 12. This claim merely details the methods of supplying voltage to the array. The method of supplying a voltage is not germane to the patentability of the circuit itself, therefore these limitations are not given patentable weight. At best these claims could be characterized as product-by-process

claims, where the process limitations are not limiting, only the structure implied by the process. See MPEP 2113. Here, the structure implied by the process steps is merely the structure of claim 12.

Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ciubotaru in view of Grodevant and further in view of Vaughan (US 2002/0186733).

With respect to claim 3, Ciubotaru and Grodevant teach the driver circuit in the rejection to claim 1, wherein the buffer circuit comprises an attenuating input stage having a pair of resistors (Ciubotaru, fig.2 R1b, R2b) and an amplifying output stage (Ciubotaru, fig.2 Abuf) including the driver amplifier to comprise a first and second amplifying transistors (Ciubotaru, fig.3 Q2m, Q3m) adapted to receive a differential input at their base (Ciubotaru, fig.3 Voutb+, Voutb-) and a load resistor connected between the collector region and voltage regulator of the second transistor (Ciubotaru, fig.3 Rout), and a common connection of the collector region of the second transistor and the load resistor adapted to provide an output to an optoelectronic device (Ciubotaru, fig.3 node below Rout). Ciubotaru and Grodevant do not teach a load resistor to be connected to the first transistor collector and voltage regulator. Vaughan teaches a driver circuit with a load resistor located between the first transistor collector region and voltage source (fig.1 #104). It would have been obvious to one of ordinary skill at the time of the invention to combine the driver circuit of Ciubotaru and Grodevant with the additional load resistor of Vaughan to enable power dissipation and load matching (Vaughan, [0027] lines 5-8).

With respect to claim 4, Ciubotaru and Grodevant teach the driver circuit in the rejection to claim 1, including the driver amplifier to comprise a first and second amplifying transistors (Ciubotaru, fig.3 Q2m, Q3m) adapted to receive a differential input at their base (Ciubotaru, fig.3 Voutb+, Voutb-) and a load resistor connected between the collector region and voltage regulator of the second transistor (Ciubotaru, fig.3 Rout), and a common connection of the collector region of the second transistor and the load resistor adapted to provide an output to an optoelectronic device (Ciubotaru, fig.3 node below Rout). Ciubotaru and Grodevant do not teach a load resistor to be connected to the first transistor collector and voltage regulator. Vaughan teaches a driver circuit with a load resistor located between the first transistor collector region and voltage source (fig.1 #104). It would have been obvious to one of ordinary skill at the time of the invention to combine the driver circuit of Ciubotaru and Grodevant with the additional load resistor of Vaughan to enable power dissipation and load matching (Vaughan, [0027] lines 5-8).

With respect to claim 5, Ciubotaru, Grodevant, and Vaughan teach the driver circuit outlined in the rejection to claim 4, and further teach the emitters of the first and second transistors to be connected to form a common node (Ciubotaru, fig.3 below Q2m &Q3m) and also that a third transistor be connected between the common node and ground (Ciubotaru, fig.3 Qmod).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ciubotaru in view of Grodevant and further in view of Vaughan and Link (US 5883910).

With respect to claim 6, Ciubotaru, Grodevant, and Vaughan teach the driver circuit as outlined in the rejection to claim 4, but do not teach a capacitor to be connected between the output voltage and ground. Link teaches a driver circuit including a capacitor between the output voltage and ground (fig.3 CAC). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the driver circuit of Ciubotaru, Grodevant, and Vaughan with the capacitor of Link in order to provide for a high pass cut-off frequency (Link, col.1 lines 63-65).

Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ciubotaru in view of Grodevant and further in view of Vaughan and Kaminishi (US 6618406).

With respect to claim 7, Ciubotaru, Grodevant, and Vaughan teach the driver circuit as outlined in the rejection to claim 4, but do not teach a compensation load to be connected coupled between the collector region of the first transistor and ground. Kaminishi teaches a driver circuit wherein a compensation load is connected between the collector region of the first transistor and ground (fig.9 Rf &Rb). It would have been obvious to one of ordinary skill at the time of the invention to combine the driver circuit of Ciubotaru, Grodevant, and Vaughan with the compensation load of Kaminishi to provide appropriate conditions for biasing the transistors into desired modes of operation (Kaminishi, col.19 lines 14-16, 42-45).

With respect to claim 9, Ciubotaru, Grodevant, Vaughan, and Kaminishi teach the driver circuit as outlined in the rejection to claim 7, but do not teach a diode to be

connected in series with the compensation load. It would have been obvious to one of ordinary skill in the art to combine the driver circuit of Ciubotaru, Grodevant, Vaughan, and Kaminishi with a diode to control current flow, as this is a widely practiced technique in the art.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ciubotaru in view of Grodevant and further in view of Vaughan and Link and Kaminishi.

With respect to claim 8, Ciubotaru, Grodevant, Vaughan, and Kaminishi teach the driver circuit as outlined in the rejection to claim 7, but do not teach a capacitor to be connected between the output voltage and ground. Link teaches a driver circuit including a capacitor between the output voltage and ground (fig.3 CAC). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the driver circuit of Ciubotaru, Grodevant, Vaughan, and Kaminishi with the capacitor of Link in order to provide for a high pass cut-off frequency (Link, col.1 lines 63-65).

Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ciubotaru in view of Grodevant and further in view of Stronczer (US 6389050).

With respect to claims 13 and 14, Ciubotaru and Grodevant teach the driver circuit in the rejection to claim 12, but do not teach the optoelectronic devices to be LEDs formed as an integrated array. Stronczer teaches a driver circuit including an array of VCSELs (fig.3 #100). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the driver circuit of Ciubotaru and Grodevant

with the array of Stronczer to provide additional outputs coupled together to achieve a higher total output power. It is also obvious to one of ordinary skill in the art to substitute LEDs for VCSELs to fit the desired application, as is a common practice in the art.

With respect to claim 15, Ciubotaru, Grodevant, and Stronczer teach the driver circuit as outlined in the rejection to claim 14, and further teach the LEDs to have their cathodes connected in common and to ground (Stronczer, fig.3 #100, caption, and is an inherent feature that the other connection (anodes) of the array will then be connected to ground in order to properly complete the circuit and allow for current flow).

With respect to claim 16, Ciubotaru and Grodevant teach the driver circuit outlined in the rejection to claim 1, but do not teach the driver amplifier to comprise a first amplifier having first and second differentially connected transistors and a first current source, and a second amplifier having third and fourth differentially connected transistors and a second current source, or a time delay network to connect between the inputs of the 2 amplifiers. Stronczer teaches a driver circuit comprising a first pair of differentially connected transistors (fig.2 T60,T50) and a first current source (fig.2 #55) and a second pair of differentially connected transistors (fig.2 T75,T80) and a second current source (fig.2 #70), and a time delay network connected between the inputs of the first and second amplifiers (fig.2 T45,T55, wherein the turn-on and switching times of the transistors provides the time delay). It would have been obvious to one of ordinary skill in the art to combine the driver circuit of Ciubotaru and Grodevant with the amplifier system of Stronczer in order to provide current mirrors to generate stable and

predictable dc reference current for biasing other circuit components (Stronczer, col.3 lines 35-38).

Allowable Subject Matter

Claims 17-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 17-21, the optoelectronic driving circuit, specifically the driver amplifier, as disclosed in the parent claims having the transistor network connections as disclosed in claims 17-21 were not found to be taught in prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tod T. Van Roy whose telephone number is (571)272-8447. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571)272-1835. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVR

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PRIMARY EXAMINER